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10/534,164	05/05/2005	Matthias Muth	DE02 0252 US	9960

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EXAMINER	
ZAMAN, FAISAL M	

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
08/23/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/534,164	MUTH, MATTHIAS	
	Examiner	Art Unit	
	Faisal M. Zaman	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 7-10** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "the digital data signal" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Claims 8-10 are rejected to a dependency on Claim 7.

Appropriate correction is therefore required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter "AAPA") and Feuerstraeter et al. (U.S. Patent Application Publication No. 2003/0058894) ("Feuerstraeter").

Regarding Claim 1, AAPA teaches a circuit comprising:

a system base chip configured for communicating over a vehicle data bus using the LIN (Local Interconnect Network) protocol, the system base chip including at least

a system voltage supply,

a system reset, and

a monitoring function (AAPA, page 2, lines 11-14).

AAPA does not expressly teach an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol, and in particular the LIN protocol, that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte, and

a serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit.

In the same field of endeavor (e.g., detection of data transfer rates in a bus system), Feuerstraeter teaches an interface circuit that, in a self-contained fashion, runs at least parts of a data bus protocol that performs detection of the bit-rate of received data, and that is capable of passing on at least one received or transmitted byte (Feuerstraeter, Figure 4, item 420, paragraphs 0044 and 0047),

A serial/parallel converter that makes use in its conversion of the bit-rate detected by the interface circuit (Feuerstraeter, Figure 3, items 350/360, paragraph 0037).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Feuerstraeter's teachings of detection of data transfer rates in a bus system with the teachings of AAPA, for the purpose of

automatically detecting a data transfer rate such that one or more devices may communicate with each other when otherwise the devices would not without using additional hardware (see Feuerstraeter, Page 1, paragraph 0011).

AAPA and Feuerstraeter disclose the claimed invention except for wherein the various components are disposed in an integrated circuit. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have disposed the components in an integrated circuit, since it has been held that forming in one piece an article which has formerly been formed in more than one piece and put together involves only routine skill in the art. *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965).

Regarding Claim 6, AAPA teaches the use of an SCI/UART (Serial Communication Interface/Universal Asynchronous Receiver Transmitter) interface (AAPA, Page 1, lines 13-17).

The motivation that was used in the combination of Claim 1, super, applies equally as well to Claim 6.

5. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Feuerstraeter as applied to claim 1 above, and further in view of Bongiorno et al. ("Bongiorno") (U.S. Patent No. 6,292,045).

Regarding Claim 2, AAPA and Feuerstraeter teach an oscillator that acts as a clock-signal source and as a timebase for the bit-rate detection (Feuerstraeter, Figure 3, items 480/490, Page 4, paragraph 0044).

AAPA and Feuerstraeter do not expressly teach wherein the oscillator is an R/C oscillator.

In the same field of endeavor (e.g., electrical circuits which use clock sources), Bongiorno teaches the use of an R/C oscillator (Bongiorno, Column 1, lines 16-21).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Bongiorno's teachings of electrical circuits which use clock sources with the teachings of AAPA and Feuerstraeter, for the purpose of providing an RC oscillator which has the ability to generate high frequency oscillations having a stable frequency characteristic.

Regarding Claim 3, Bongiorno teaches wherein the clock signal generated by the R/C oscillator may also be provided to circuits outside the integrated circuit, and in particular to a microprocessor (Bongiorno, Column 1, lines 16-21).

The motivation that was used in the combination of Claim 2, super, applies equally as well to Claim 3.

6. **Claims 4 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Feuerstraeter as applied to Claim 1 above, and further in view of Werle (U.S. Patent No. 5,778,002).

Regarding Claims 4 and 5, AAPA and Feuerstraeter do not expressly teach wherein the interface circuit may also pass on complete messages and perform buffer-storage of data received or to be transmitted.

In the same field of endeavor (e.g., multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation), Werle teaches wherein an interface circuit may pass on complete messages by performing buffer-storage of data received or to be transmitted (Werle, Figure 1, item 14, Column 3, lines 13-27).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Werle's teachings of multiplexing asynchronous high-speed and low-speed data into a single data stream for recordation with the teachings of AAPA and Feuerstraeter, for the purpose of reducing latency of the system if the incoming data rate is slower than that which can be processed.

7. **Claims 7-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pohlmeyer et al. (U.S. Patent No. 6,959,014) ("Pohlmeyer"), Jeter (U.S. Patent No. 4,951,776), and Feuerstraeter.

Regarding Claim 7, Pohlmeyer discloses an integrated circuit comprising:

a base chip including one or more circuits (Pohlmeyer, Figure 1, item 100) configured to

receive a vehicle battery voltage (Pohlmeyer, Column 2, lines 21-28);

receive analog signals from a serial communication interface/universal asynchronous receiver transmitter (SCI/UART) interface (Pohlmeyer, Column 2, lines

12-13), the analog signals corresponding to data formatted for a Local Interconnection Network (LIN) protocol (Pohlmeyer, Column 3, lines 23-25);

identify individual bytes from the digital data signal (Pohlmeyer, Figure 2, item 200, Column 3, lines 23-33);

identify a LIN protocol header from at least one of the individual bytes (Pohlmeyer, Column 3, lines 23-33);

detect a bit rate for the received analog signals in response to the detected LIN protocol header and with reference to a clock signal (Pohlmeyer, Column 4, lines 1-8); and

convert the analog signals to a digital data signal in response to the detected bit rate (Pohlmeyer, Column 2, lines 21-28).

Pohlmeyer does not expressly disclose the steps of convert the vehicle battery voltage to a regulated voltage;

provide the regulated voltage as an output of the integrated circuit;

monitor the vehicle battery voltage;

provide a reset signal in response to the monitoring of the vehicle battery voltage;

perform a serial to parallel conversion on the digital data signal; and

provide the parallel-converted digital data signal as an output of the integrated circuit.

In the same field of endeavor (e.g., vehicle data communications), Jeter teaches the steps of convert a vehicle battery voltage to a regulated voltage (Jeter, Figure 5, item 92, Column 5, lines 54-58);

provide the regulated voltage as an output of an integrated circuit (Jeter, Figure 5, item SCO, Column 5, lines 21-42);

monitor the vehicle battery voltage; and

provide a reset signal in response to the monitoring of the vehicle battery voltage (Jeter, Column 4, lines 59-63).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Jeter's teachings of vehicle data communications with the teachings of Pohlmeyer, for the purpose of assuring proper voltage levels within the integrated circuit.

Also in the same field of endeavor (e.g., automatic data rate detection techniques), Feuerstraeter teaches the steps of perform a serial to parallel conversion on a digital data signal (Feuerstraeter, Figure 5, item 505; i.e., incoming data signal DIP/DIN); and

provide the parallel-converted digital data signal as an output of the integrated circuit (Feuerstraeter, Figure 5, items RXDATA0P/RXDATA0N - RXDATA15P/RXDATA15N).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Feuerstraeter's teachings of automatic data rate detection techniques with the teachings of Pohlmeyer, for the purpose of being able to process multiple signals simultaneously.

Regarding Claim 8, Feuerstraeter and Pohlmeyer teach wherein the one or more circuits are further configured to receive data from a parallel bus input to the integrated circuit (Feuerstraeter, Figure 5, item 504);

convert the data from the parallel bus input to a serial form (Feuerstraeter, Figure 5, item OUT/OUTN); and

transmit the serial form of the data from the parallel bus input on the SCI/UART (Pohlmeyer, Column 2, lines 12-13) interface in response to the detected bit rate (Feuerstraeter, paragraph 0037).

The motivation that was used in the combination of Claim 7, supra, applies equally as well to Claim 8.

Regarding Claim 9, Pohlmeyer discloses wherein the one or more circuits are further configured to provide a watchdog function and in response to the watchdog function provide an interrupt as an output of the integrated circuit (Pohlmeyer, Column 6, lines 29-41).

Regarding Claim 10, Pohlmeyer discloses wherein the base chip further includes a resistor- capacitor (RC) clock generation circuit that is configured to provide the clock signal (Pohlmeyer, Column 4, lines 5-15).

Response to Arguments

8. Applicant's arguments filed 7/28/2010 have been fully considered but they are not persuasive.

Regarding Claim 1, Applicant argues that "the '894 reference does not teach a single integrated circuit package." However, as discussed in the rejection above, it would have been obvious to one of ordinary skill in the art to dispose the various claimed components into an integrated circuit, since it has been held that forming in one piece an article which has formerly been formed in more than one piece and put together involves only routine skill in the art. *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965). Furthermore, in response to Applicant's arguments, the recitation "integrated circuit" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Therefore, Applicant's arguments with respect to this limitation are not persuasive.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal M. Zaman whose telephone number is 571-272-

6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm, alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Faisal M Zaman/
Patent Examiner, Art Unit 2111